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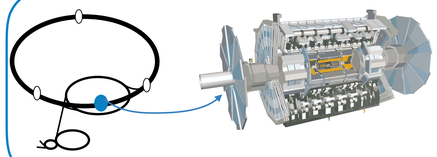
Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Maheyer J. Shroff
on behalf of the ATLAS Liquid Argon Calorimeter Group

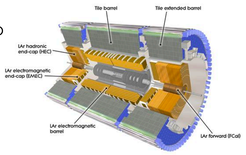
ATLAS EXPERIMENT
University of Victoria

ATLAS....



ATLAS is a general-purpose detector used to study particles produced by high-energy proton-proton collisions at the LHC.

... the LAr Calorimeter



- Consists of a Sampling Calorimeter with LAr as sampling medium.
- Signal amplified, shaped and digitized at 40 MHz.
- 182,500 channels.

... and the HL-LHC

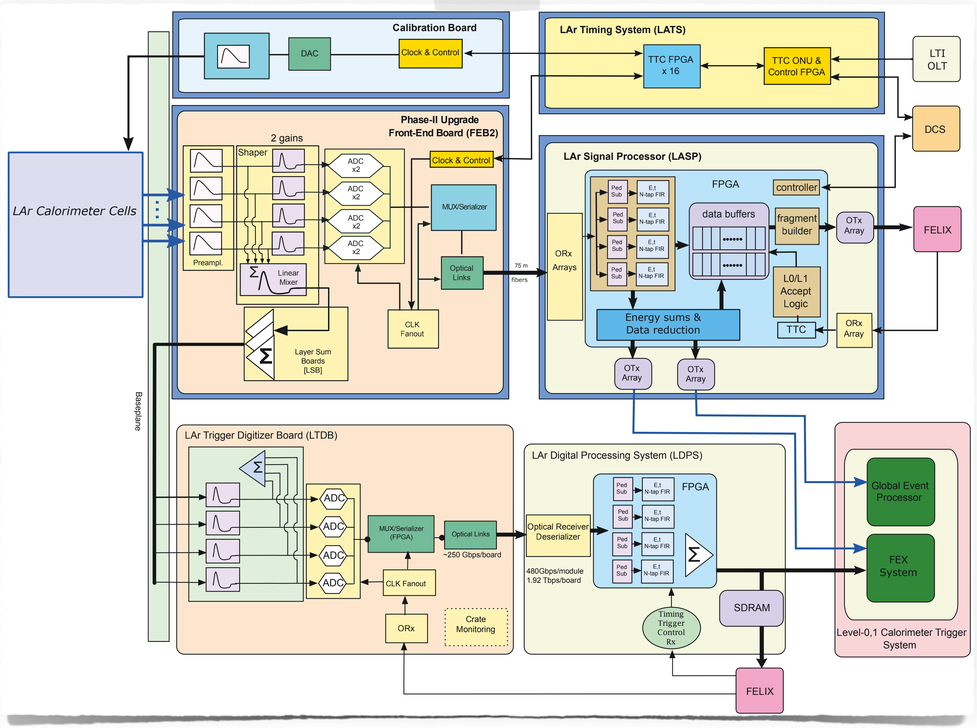
The LHC is due to undergo the Phase-II Upgrade in 2025-2027 $\Longrightarrow$ **HL-LHC.**

Instantaneous luminosity up to 5 to 7 x nominal with $< \mu > \approx 140 - 200$.

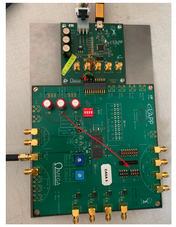
An integrated luminosity of up to 4000 fb^{-1} is planned to be achieved after 12 years.

- To differentiate signal from noise, higher granularity shower information needs to be sent to the trigger.
- ATLAS TDAQ system will evolve to a trigger rate of 1 MHz
- High Radiation dose to front-end electronics.
- As a result, the LAr Calorimeter readout needs to be upgraded as well.
- Requires new On- and Off-detector components for the LAr calorimeter (to feed trigger and DAQ systems)

Phase-II Upgrade



Calibration Board



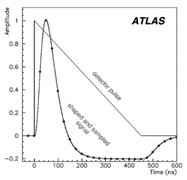
Objective:
- Injects a pulse of known amplitude and shape directly on calorimeter cells for 128 channels
- Must cover full dynamic range: 320 mA, up to 7.5 V output: requires HV-CMOS

Status: Pulser and DAC ASICs
CLAROCv3 Pulser ASIC
- Based on XFAB HV-CMOS 180 nm technology
- 4 calibration channels

LADOCv1 16-bit DAC ASIC
- Based on TSMC 130 nm CMOS technology

- *32-channels boards (CABANON) are being tested since June*
- *Final ASIC prototype planned for end of year*

Preamplifier - Shaper



Objective:
- Amplifies and applies a CR-(RC)2 shaping function and splitting to 2 overlapping gains
- Large dynamic range: 10 mA for 25 Ω channels and 2 mA for 50 Ω channels
- Noise: < 350 nA for 10 mA channels, <120 nA for 2 mA channels, INL < 0.2%

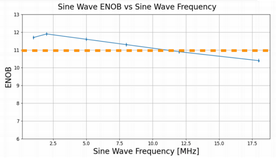
Status: ALFE1 ASIC
- Based on 130 nm CMOS technology
- TID tests demonstrated sufficient radiation tolerance

- *Submitted for fabrication*

ADC

Objective:
- Digitizes analog signals at 40 MHz on two gains
- 14-bit dynamic range with >11-bit precision

Status: COLUTAv3
- Fully custom based on 65 nm CMOS technology
- 40 MHz pipeline ADC with Multiplying DAC (MDAC) in combination with a 12-bit pipeline Successive Approximation Register (SAR) ADC



- Achieves 11.7 and 11.3 Effective Number of Bits (ENOB) at 1 and 8 MHz respectively
- Meets power consumption and radiation hardness requirements

- *COLUTAv4 design to be submitted by the end of summer 2021*

LAr Timing System

Objective:
- Distributes Trigger, timing and control (TTC) signals to FEBs and Calibration boards

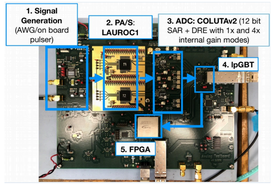
Status: LATOURNETTE
- One central and 12 matrix Cyclone10 GX FPGAs
- *Power tree of the board is designed*
- *First PCBs being assembled*

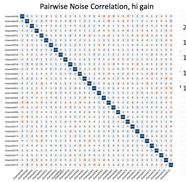
Front End Board

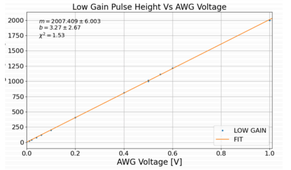
Objective:
- Integrates PA/S, ADC and optical links
- 1 FEB2 board handles 128 channels

Status: Prototype - Analogue testboard
- 2 channels with Pre-Prototype ASICs
- Full readout chain working

Status: Prototype - FEB2 slice testboard
- 32 channels with updated ASICs
- Functionality of full readout chain and multi-channel performance demonstrated with noise, sine wave, and pulse measurements
- Correlation of noise now within specification





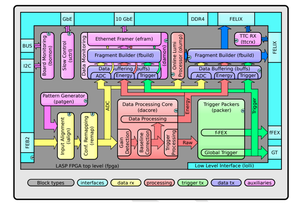


LAr Signal Processor

Objective:
- Receives digitized waveform from 8 FEB2s
- Determines energy and timing of signals for up to 1024 channels at up to 1.8 Tbps
- Output data at 200 Gbps to the Global Event Processor and to the fFEX at up to 1 Tbps
- Sends data, energy and timing to the DAQ at 60 Gbps upon receiving a trigger accept

Status: LASP Board
- Implemented using 2 Intel Stratix-10 FPGAs
- Test board design complete and Power DC simulation done
- *First fully assembled boards expected by end of Summer 2021*

LASP Firmware



- All FW components meet at least minimal entity design
- Successful injection of emulated ADC data with lpGBT/VTRX+ testboard
- Studies ongoing on the clock distribution as well as the resource segmentation

Picture References: CERN-LHCC-2017-018