Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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ATLAS EXPERIMENT

CERN

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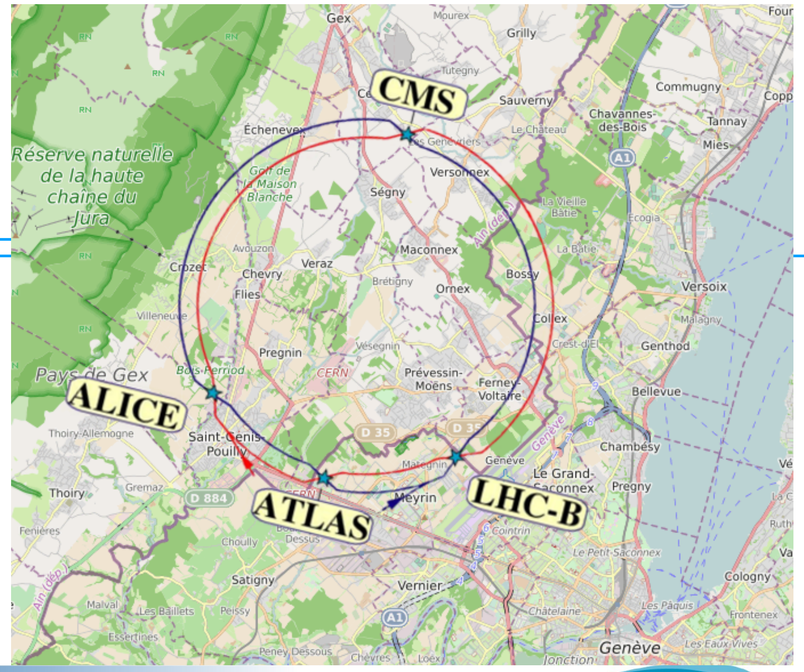
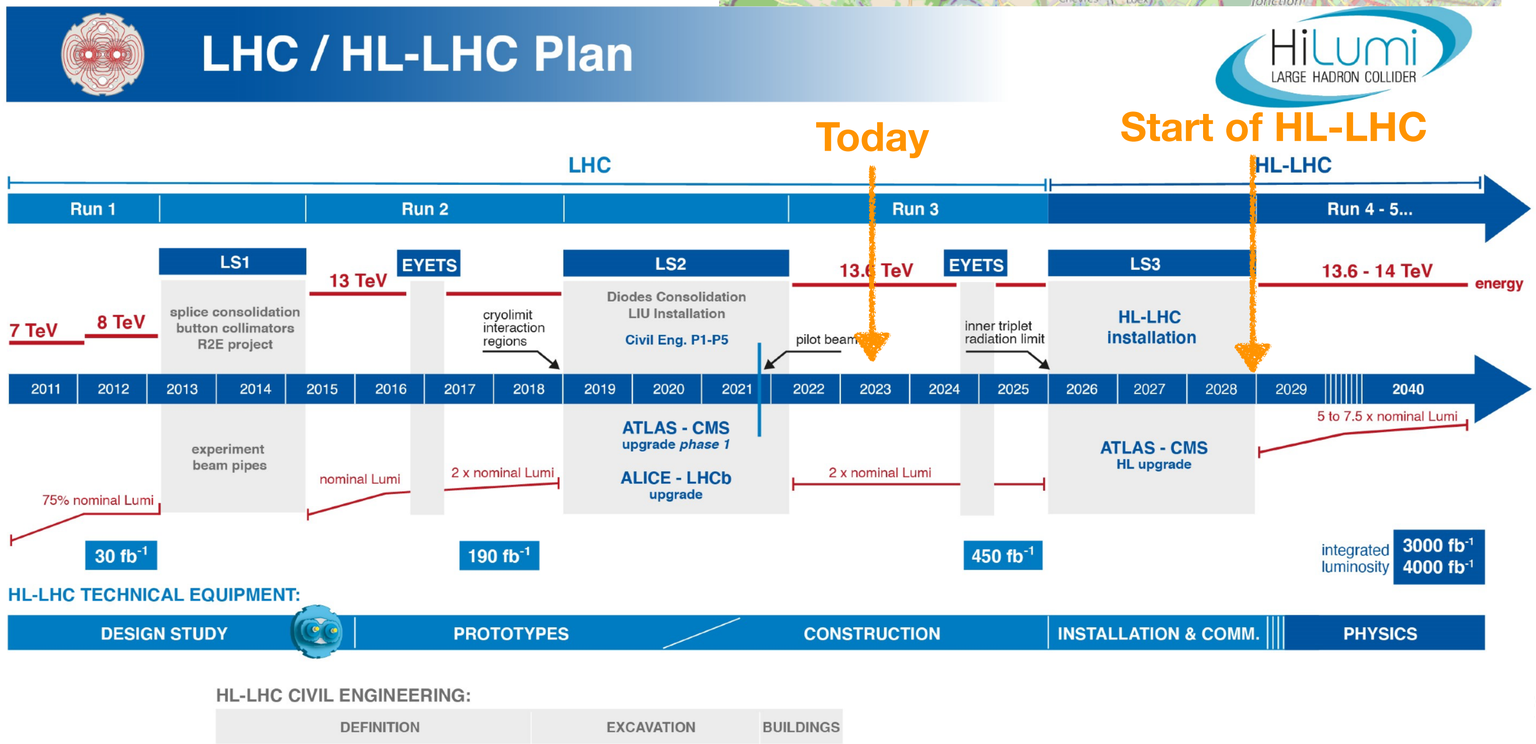
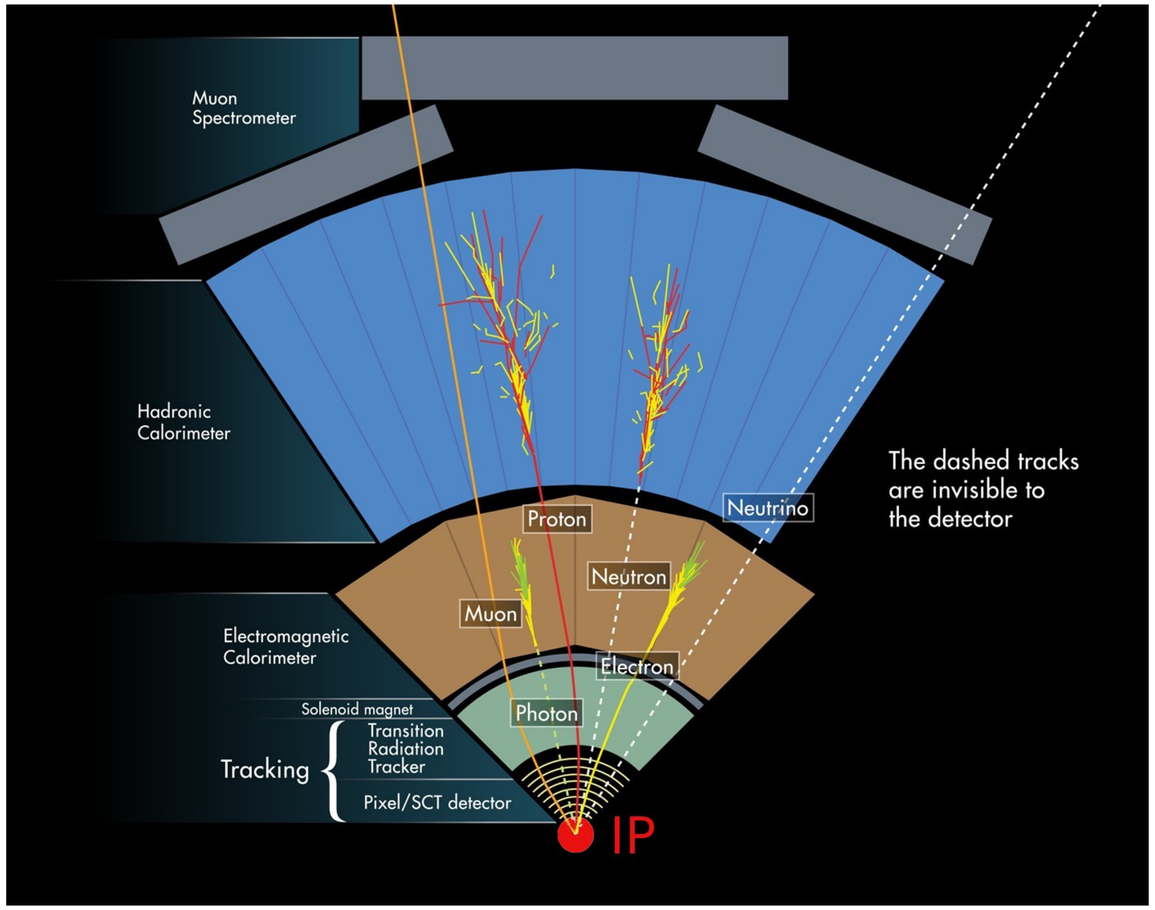
Toward HL-LHC

- The LHC will have a major upgrade during the next long shutdown in 2026-2029; will become High Luminosity LHC
- The goal is to reach and instantaneous luminosity up to 7×10^{34} cm^{-2} s^{-1} (~7 times the design value)
- Up to 200 proton-proton interactions will occur every 25 ns
- Should allow to record 10 times more data in the following decade than what have been done so far
- Would allow to probe even further the standard model and especially rare processes.



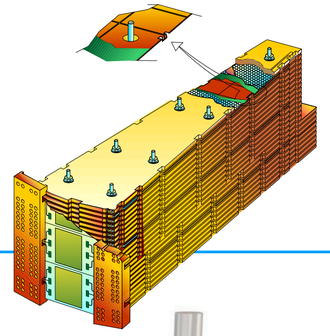


ATLAS experiment

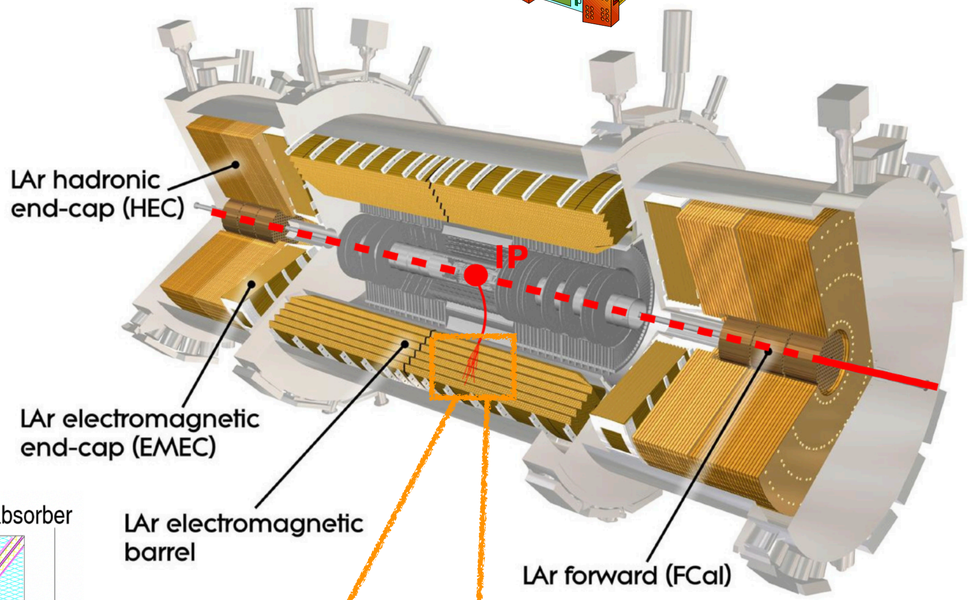


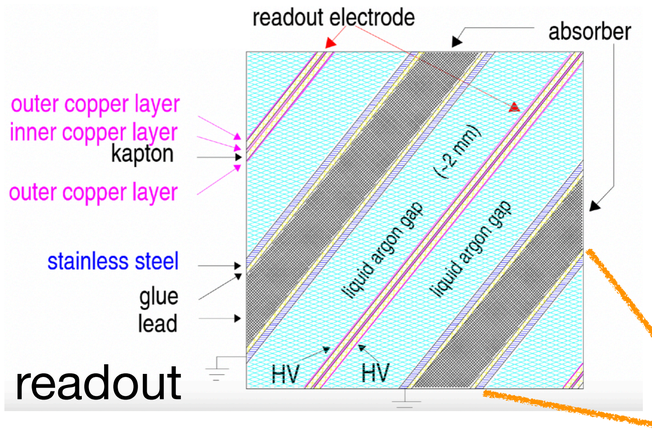
- Large multipurpose experiment at one of the colliding points of LHC
- Built for new physics search and precision measurement of the Standard Model of particle physics
- Structured by layers of sub-detectors
    1. Inner tracker
    2. Electromagnetic calorimeter
    3. Hadronic calorimeter
    4. Muon spectrometer
- Can detect and measure the energy and positions of electrons, photons, muons and jets
- Neutrinos are not directly measured but estimated by reconstruction of missing transverse energy

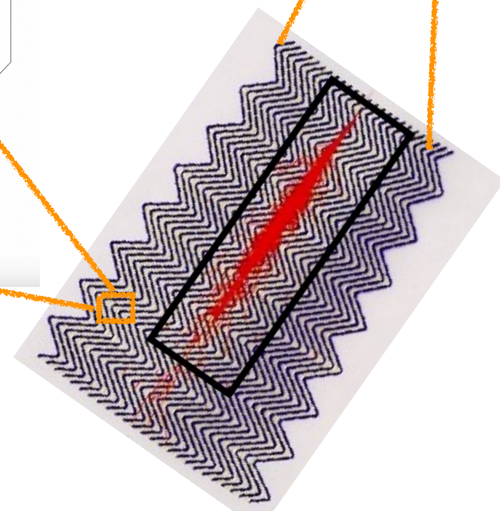
Liquid Argon Calorimeters (LAr)

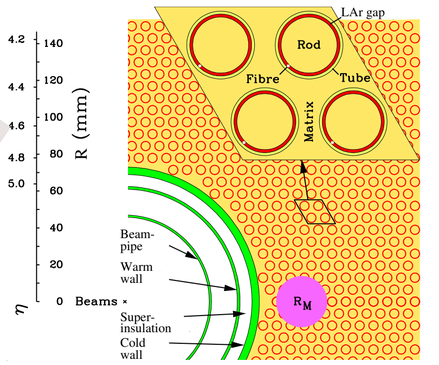


- Used for electromagnetic calorimetry in central and forward regions and hadronic calorimetry in forward regions
- Sampling calorimeter with liquid argon as active material and lead, copper and tungsten as passive material
- Accordion geometry for electromagnetic calorimetry ($|\eta| < 3.2$) to ensure full azimutal coverage
- Copper plates for hadronic calorimeter in forward regions ($1.5 < |\eta| < 3.2$)
- Honeycomb structure for very forward regions ($3.1 < |\eta| < 4.9$)
- **Total of 182k units of readout**
- Provide data for both trigger and precision readout



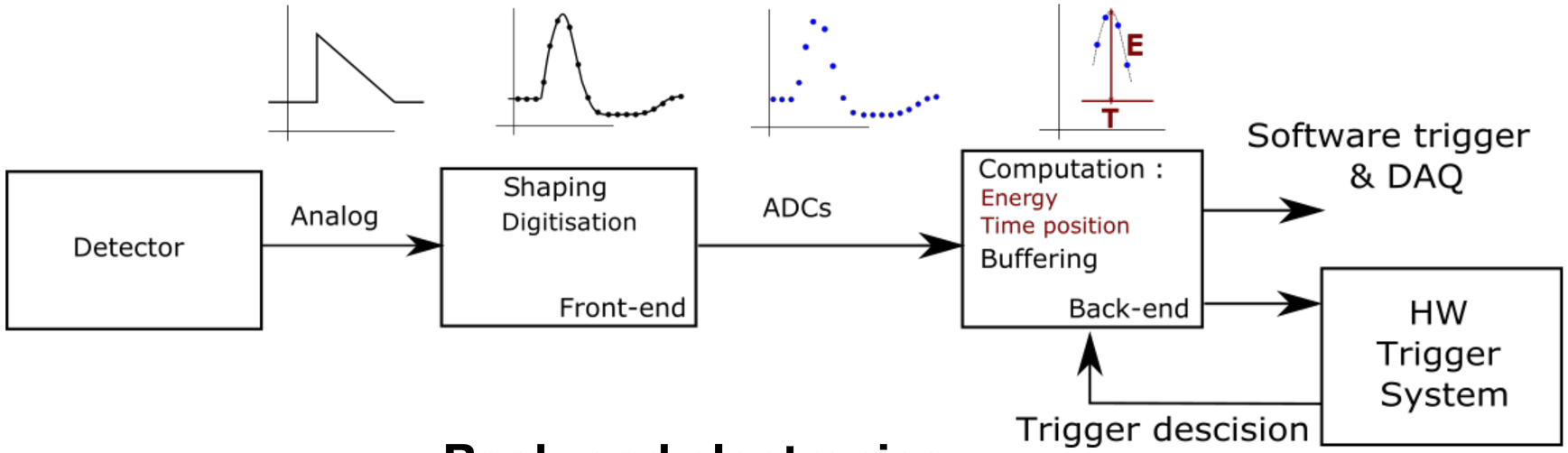






LAr Readout principles for HL-LHC

- A triangular pulse is generated when a particle deposits energy in the detector



Front-end electronics

- The signal is shaped to a bipolar pulse
- Pulse is sampled and digitised at 40 MHz
- Digits are sent via optical link to the back-end system

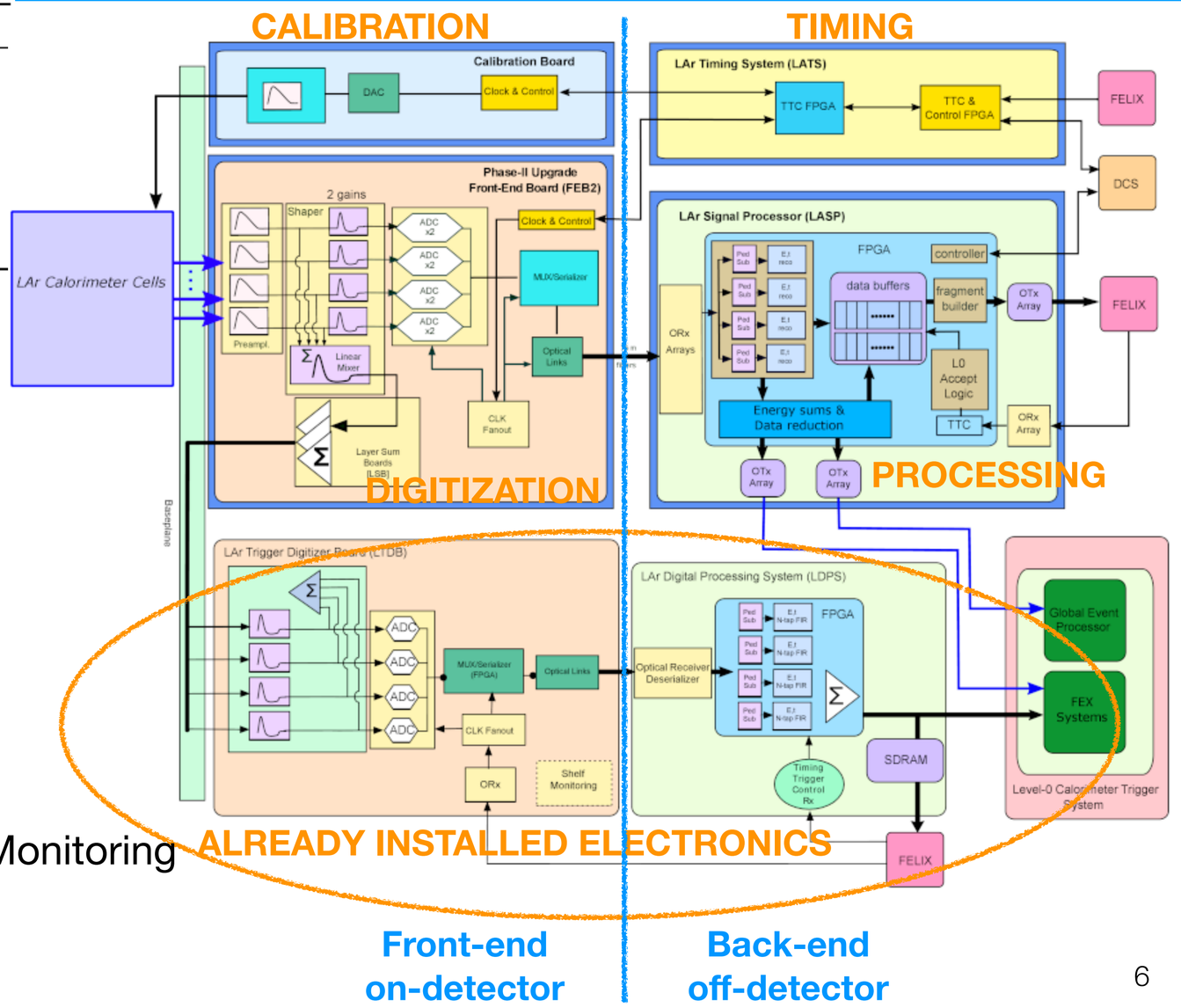
Back-end electronics

- Process the digits to extract energies values for each cell
- Compute also time position of the pulse
- Send energies values at 40 MHz to the trigger system
- Buffer data before trigger decision
- Send full precision data stream to data acquisition

LAr upgrade for HL-LHC

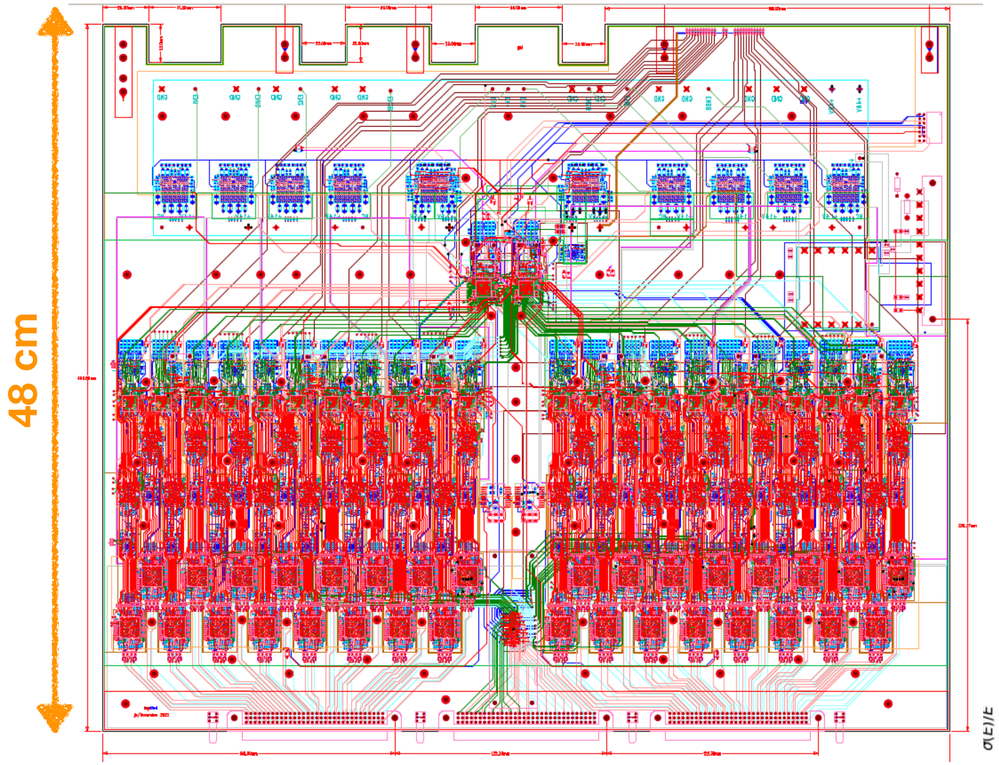
	TID [kGy]		NIEL [n_{eq}/cm^2]		SEE [h/cm^2]	
ASIC	2.26	(2.25)	4.9×10^{13}	(2)	7.7×10^{12}	(2)
COTS (multiple lots)	30.2	(30)	19.6×10^{13}	(8)	3.1×10^{13}	(8)
COTS (single-lot)	7.5	(7.5)	4.9×10^{13}	(2)	7.7×10^{12}	(2)
LVPS between TileCal fingers (barrel)	6.0	(30)	4.4×10^{13}	(8)	8.0×10^{12}	(8)
LVPS at PP2 (barrel)	0.39	(30)	2.4×10^{12}	(8)	3.4×10^{11}	(8)
LVPS between TileCal fingers (endcap)	4.26	(30)	9.8×10^{12}	(8)	1.5×10^{12}	(8)
HEC LVPS	0.32	(2.25)	2.4×10^{12}	(2)	3.8×10^{11}	(2)

- Higher luminosity induce significant increase of the radiation dose
  - Legacy front-end electronic to be replaced
- Profit from latest technologies
- Should cope with higher trigger rates
- 4 main components to be re-worked:
  - Shaping + Digitization
  - Processing
  - Calibration
  - Timing + Control + Monitoring



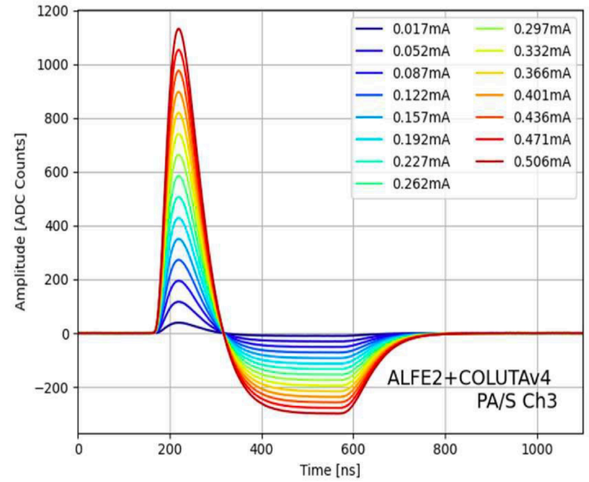
Digitization & Shaping boards (FEB2)

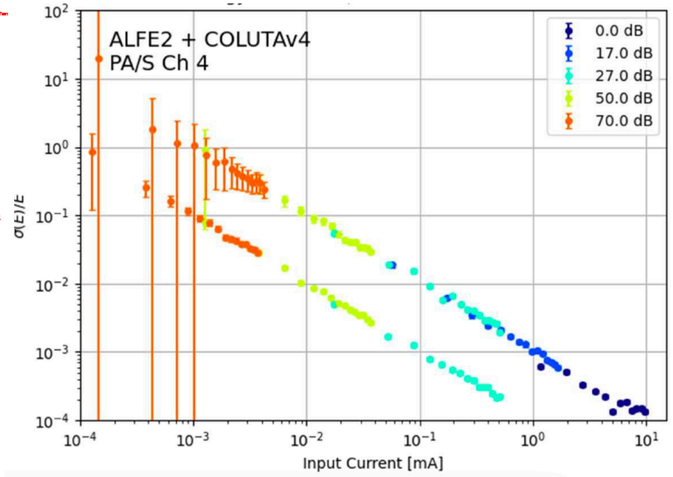
- Custom ASICs Design :
  - ALFE: custom 130 nm CMOS ASIC
    - preamp-shaping CR-$(RC)^2$
    - **2 gains**
  - COLUTA: custom 65 nm CMOS ASIC
    - Rad-hard ADC
    - **>11 bits precision and 14 bits of dynamic range**
- Front-End Board (FEB2) prototype in preparation with :
  - Latest version of ASICs
  - Full scale number of with **128 channels**
  - Work ongoing to finalise rad-hard powering



Design of fully equipped board
- **32 Preamp-shaper (ALFEs)**
- **32 ADCs (COLUTAs)**
- **22 serializer (lpGBT)**

1524 FEB2 will be mounted on the detector

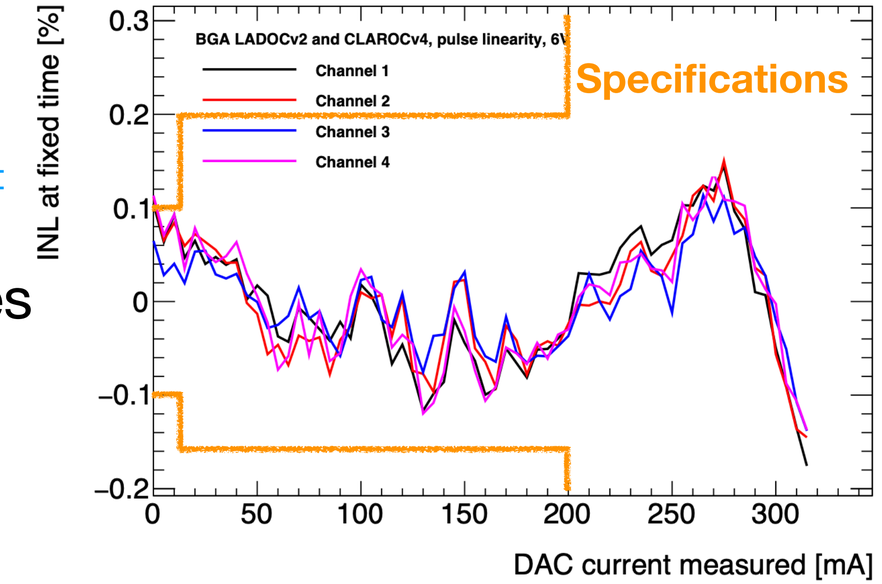


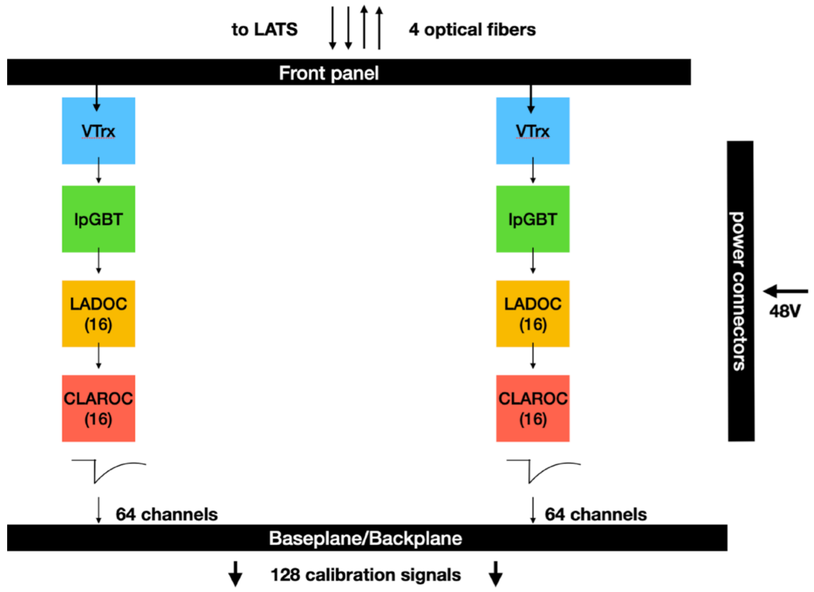


Energy resolution

Calibration boards

- Inject known pulse into the cryostat for calibration purposes
- Needed 2 custom mades ASIC
  - CLAROC: HF Switch 180 nm XFAB
  - LADOC: 130 nm CMOS ASIC for 16b DAC
- Very good pulse linearity over the full expected range
- Radiation hardness under test
- Full scale board in preparation
- **122 calibration** boards will be mounted on the detector



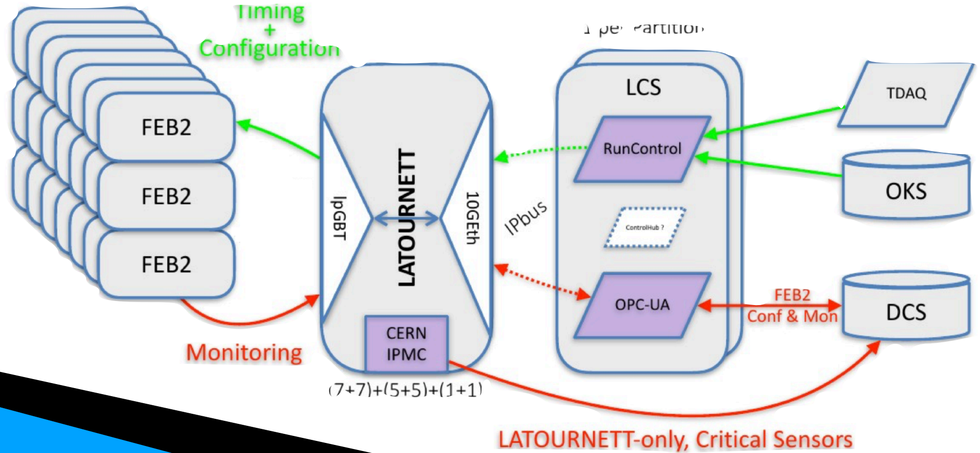


Full scale board diagram

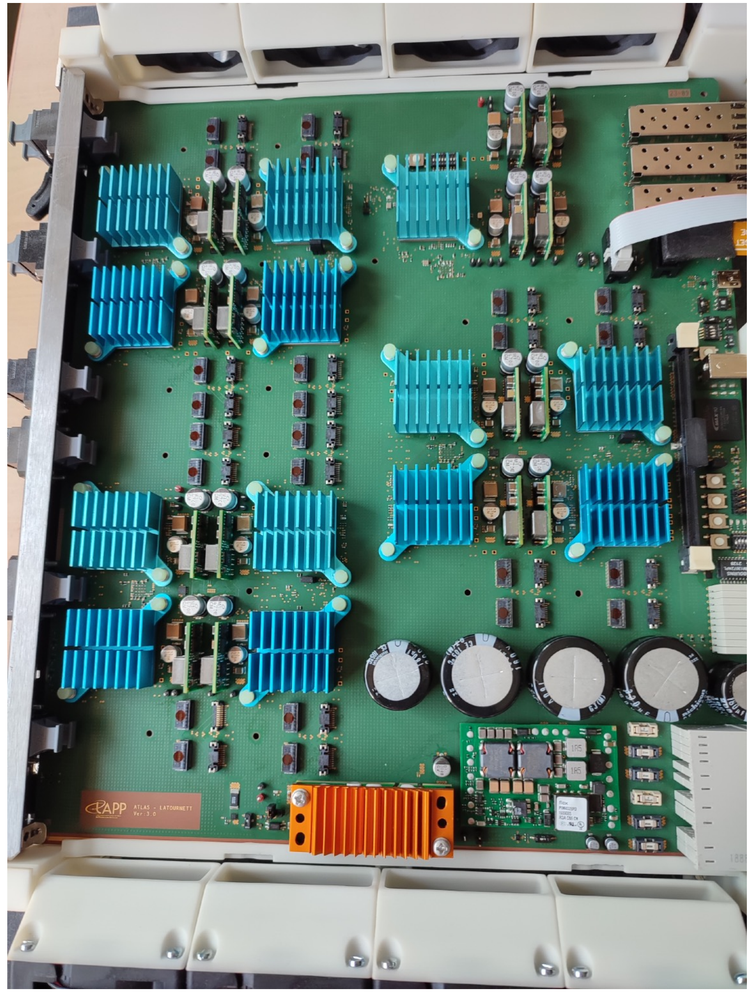
Timing/Control/Monitoring boards

- LATOURNETT board for time control and monitoring of front-end
- ATCA board with High 13 FPGA (1 master and 12 slaves)
- Each LATOURNETT could control up to 72 front-end boards
- Should transmit both timing an control commands to front-end via Rad-hard lpGBT protocol through optical links
- Ethernet commands (asynch. with LHC) and timed-in signals (synch. with LHC) are merged into a single synch. lpGBT frame
- 30 boards will be for the whole detector
- Clock jitter < 1 ns at the front-end level

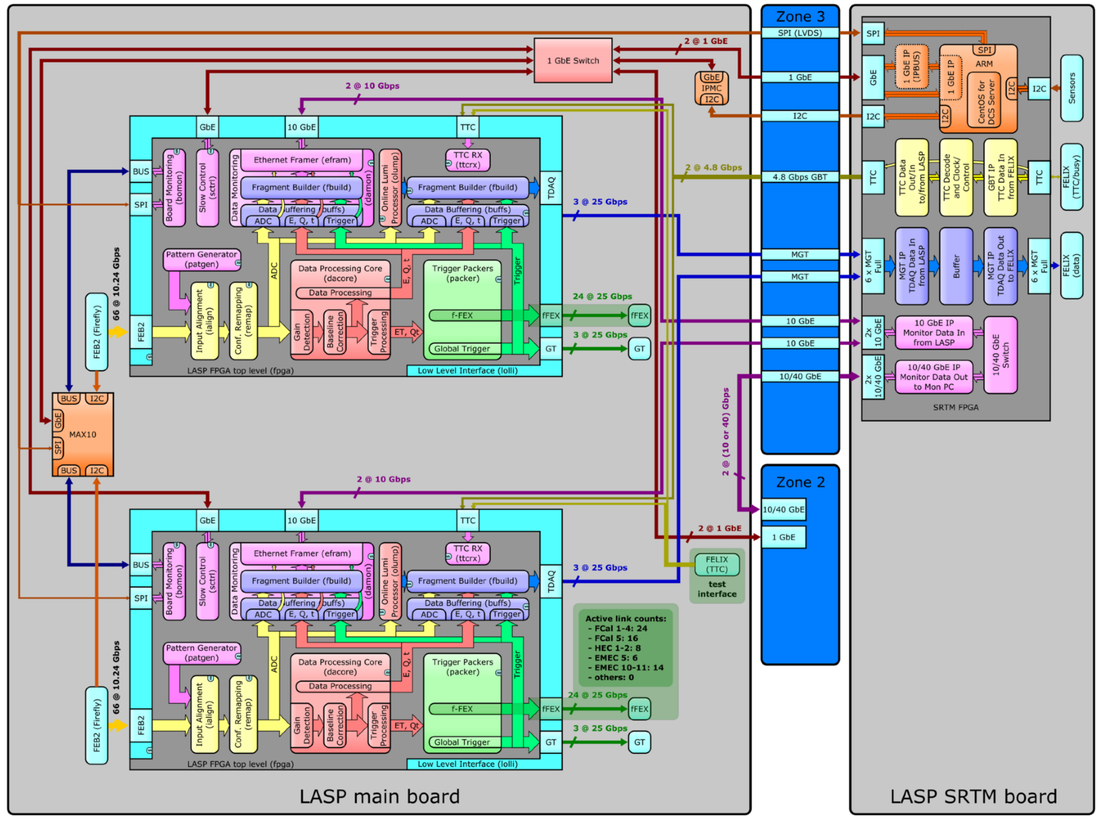
Integration principle of the timing and control system



Prototype of LATOURNETT board



Data processing board (LASP)

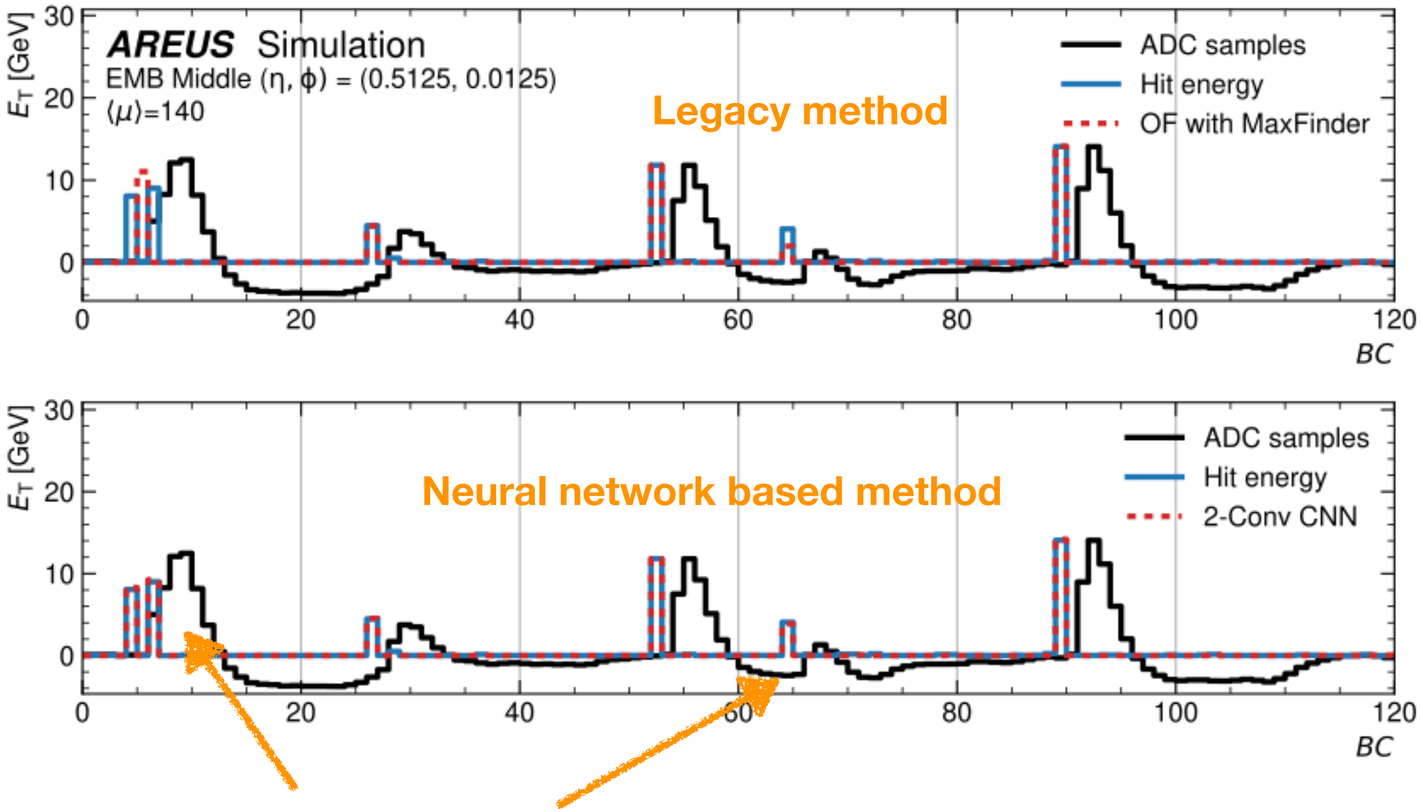


Detailed schematics of the firmware blocks and main signal paths on the processing boards

- The processing board (LASP) receive ADCs from up to 6 FEB2 and process energies values out of them for each LHC bunch crossing (40 MHz)
- ATCA board with 2 large FPGA (AGILEX) + Smart Rear Transition Module (SRTM) with a SOC (Zynq)
- The 278 boards should in total receive and process an amount of **0.34 Pbps.**
- Rad-hard lpGBT protocol used for data transmission from detector
  - Up to 132 links @10.24 Gbps for each board
- Should provide energy values @40 MHz for trigger decision
- Should buffer data for ~10 μs before sending it to DAQ
- Very complex firmware under development to meet all those requirements

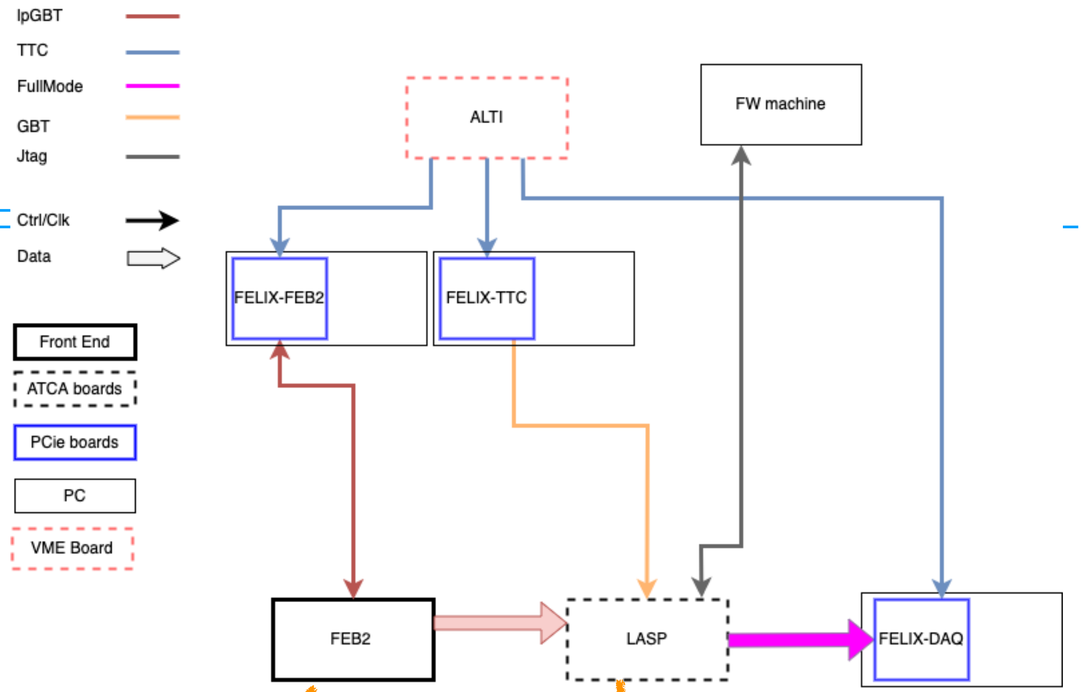
Online energy computation

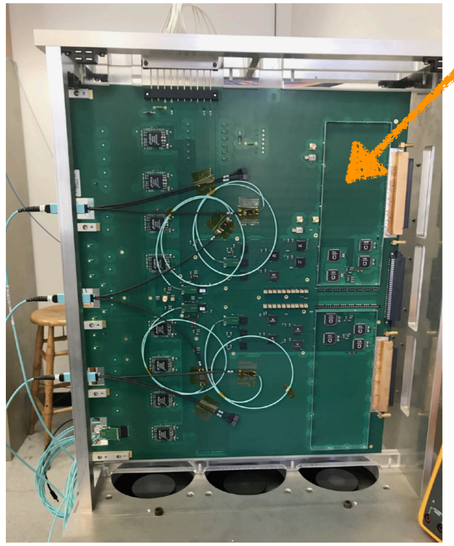
- There is more in Anne-Sophie's talk
- With higher luminosity more particle will deposit energies on the detector
- More chance to have pulse close in time in a single readout channel
  - Current method of Optimal Filtering is not sufficiently precise anymore
- Plan to used advanced neural network algorithms embedded in FPGA to compute the energies in such harsh conditions



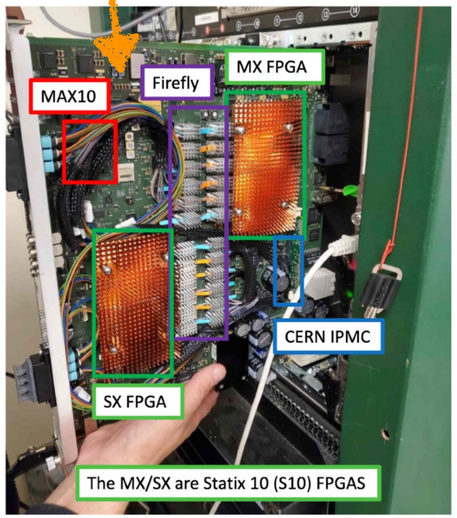
Integration & Tests

- Integrated within a “mini” readout chain have been built at CERN
  - 32 channels digitizer (FEB2) test board
  - Processor (LASP) test board with previous generation of FPGA
  - Services (timing/control/readout) based on legacy hardware
- Now preparation of a “medium” readout chain
  - 14 FEB2 read simultaneously
- Installation on ATLAS detector to start in 2027





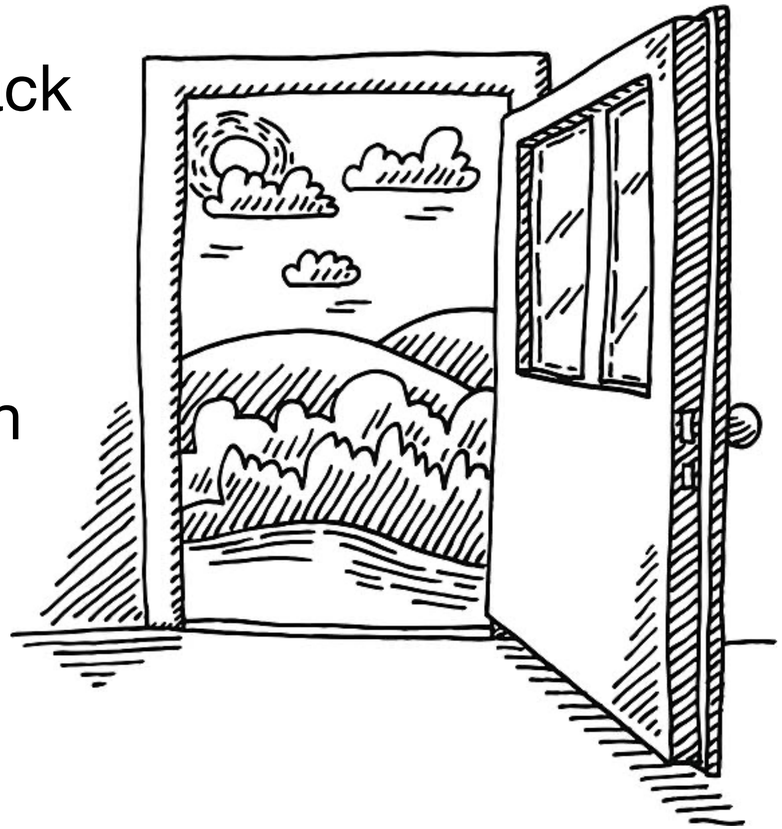
FEB2 (Digitizer) test board with 32 channels



LASP (processor) test board

Summary

- Liquid argon calorimeter upgrade for HL-LHC is on track
- ASICs for front-end boards have been validated and production has started
- Full scale prototype boards of each type in preparation
- First integration test demonstrated successful communication between boards
- More achievements expected soon!



Backup

References

- ATLAS Document
- Phase-2 scoping document
- Liquid Argon Calorimeter Phase-2 Technical design report